

What is claimed is:

1. A solid-state image sensor having a readout architecture that incorporates charge multipliers, said image sensor including:

a first CCD register adjacent to at least a second CCD register and coupled to the said first register through a charge overflow barrier.

2. The image sensor according to claim 1 wherein the second adjacent CCD register collects overflow charge and transports it to at least one detection node located in each register, and

each charge conversion node having charge conversion sensitivity that may be different for each node.

3. The image sensor according to claim 2, wherein signals from adjacent register detection nodes are processed and combined according to a predetermined mathematical formula.

4. A solid-state image sensor having a readout architecture that incorporates charge multipliers, said image sensor including:

a CCD register that incorporates at least one charge-multiplication device element in at least one stage and said at least one stage has a progressively wider width.

5. The image sensor according to claim 4, wherein the width of the CCD register-stages and the number of charge-multiplication elements in at least some of its stages varies according to a predetermined formula.

6. The image sensor according to claim 5, wherein the predetermined formula has an exponential dependency on the number of CCD stages that include charge multiplication devices.

7. The image sensor according to claim 4, wherein the CCD register includes a clearing gate and a clearing drain to remove unwanted charge.

8. The image sensor according to claim 4, wherein the CCD register has a charge overflow barrier and a charge overflow drain incorporated in at least one of its stages to prevent charge blooming.

9. A solid-state image sensor having a readout architecture, said readout architecture incorporating:

charge multipliers;

CCD registers; and

a charge overflow device in at least one of its registers.

10. The image sensor according to claim 4, wherein the sensor is oriented in a one crystallographic direction on the semiconductor substrate, and wherein the charge flows in said one direction through a high electrical field to minimize charge multiplication noise.

Year	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	